REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed November 1, 2005.

Currently, claims 1-44 and 52-53 are pending.

I. Allowable Subject Matter

In paragraph 5 of the Office Action, the Examiner indicated that claim 6 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. In accordance with the Office Action, Applicant has rewritten claim 6 to be in independent form and to include the limitations of independent claim 1. Therefore, Applicant asserts that claim 6 is in condition for allowance. Based on their dependency from claim 6, Applicant asserts that claims 7-9 and 52-52 are also in condition for allowance.

II. Response to Rejections

The Examiner rejected claims 1-3, 5, 10-21, 25-31 and 35-44 under 35 U.S.C. §103(a) as being unpatentable over Hazani in view of Forbes. Because neither reference, alone or in combination, teaches or suggest all of the limitations of the claims, Applicant asserts that claims 1-3, 5, 10-21, 25-31 and 35-44 are in condition for allowance.

One embodiment of Applicant's non-volatile storage device includes two dielectric regions. A first dielectric region is between the floating gate and the channel region. A second dielectric region is between the floating gate and the control gate. The dielectric region between the floating gate and the channel region includes high-K material. The dielectric region between the floating gate and control gate is used to transfer charge between the floating gate and control gate. The combination of the dielectric region between the floating gate and the channel region including high-K material and the dielectric region between the floating gate and control gate being used to transfer charge between the floating gate and control gate is recited in Applicant's claims and not taught or suggested by the prior art.

For example, claim 1 recites:

a first dielectric region between said channel region and said floating gate, said first dielectric region includes a high-K material; and

a second dielectric region between said floating gate and said control gate, wherein charge is transferred between said floating gate and said control gate via said second dielectric region.

Claim 30 recites:

said floating gate being separated from said channel by a first dielectric region that includes a high-K material, said floating gate being separated from said control gate by a second dielectric region ... said control circuit causes charge to be transferred between said floating gate and said control gate via said second dielectric.

Independent claims 20, 29 and 39 have analogous limitations.

The cited prior art does not teach the combination of the dielectric region between the floating gate and the channel region including high-K material and the dielectric region between the floating gate and control gate being used to transfer charge between the floating gate and control gate, as recited in Applicant's claims.

Hazani discloses an EEPROM cell:

The cell includes a p- substrate 25. Two n+ diffused regions 28a and 28b are spaced apart by a channel 34. An oxide layer 29 covers regions 28a and 28b. The drain area 34a of the channel is covered with an oxide layer 29a and a polycrystalline silicon layer 30. The source area 34b of the channel is covered by a thermal oxide layer 31. Thermal oxide layer 31 is covered by and disposed under a deposited TEOS oxide layer 32 which is thicker than thermal oxide 31. Polycrystalline silicon layer 33 is disposed over deposited oxide layer 32. Oxide layer 29 is greater in thickness over the n+ diffused regions 28a and 28b that are not overlapped by the floating gate 30 than the thickness of oxide layer 29a over the drain area 34a of the channel. Silicon dioxide layers 31 and 32 isolate the polycrystalline region 30 and the polycrystalline layer 33. Polycrystalline layer 33 that is disposed over the upper surface of

> oxide layer 32 over the source area 34b of the channel 34 and also disposed over the upper surface of oxide layer 32 over the polycrystalline region 30. The deposited TEOS-silicon dioxide layer 32 is directly disposed over and is in contact with thermal oxide layer 31. Thermal silicon dioxide layer 31 is disposed over and is in contact with the source area 34b, oxide layer 31 is also disposed over and is in contact with the polycrystalline floating gate layer 30. The channel region 34 of the cell is integrally formed between the n+ regions 28a and 28b. The n+ regions 28a and 28b form the drain and the source of the transistor respectively. A floating gate 30 is formed by the polycrystalline silicon region 30 over the drain area 34a of the channel. The control gate is formed by the polycrystalline silicon 33 over the source area of the channel 34b and over the floating gate 30. [Hazani, col. 10, lines -31]

Hazani does not teach or suggest "a first dielectric region between said channel region and said floating gate, said first dielectric region includes a high-K material; and a second dielectric region between said floating gate and said control gate, wherein charge is transferred between said floating gate and said control gate via said second dielectric region," as recited in claim 1.

Forbes discloses a flash memory device with a high-K dielectric between the floating gate and the channel. However, rather than transfer charge via the dielectric between the floating gate and the control gate, Forbes teaches to transfer charge via the high-k dielectric between the floating gate and the channel. This is a significant difference as compared to Applicant's claims. Therefore, Forbes does not teach or suggest "a first dielectric region between said channel region and said floating gate, said first dielectric region includes a high-K material; and a second dielectric region between said floating gate and said control gate, wherein charge is transferred between said floating gate and said control gate via said second dielectric region," as recited in claim 1.

Combining Hazani and Forbes also does not teach or suggest "a first dielectric region between said channel region and said floating gate, said first dielectric region includes a high-K material; and a second dielectric region between said floating gate and said control

gate, wherein charge is transferred between said floating gate and said control gate via said second dielectric region," as recited in claim 1.

Rather, Forbes teaches to use the high-K dielectric to transfer charge. Thus, any combination with Forbes would have the charge transferred via the high-K dielectric, which is different than the above-quoted language from Applicant's claims which requires transfer of charge via the other dielectric.

Applicant further asserts that there is no motivation to combine and alter the prior art to create the invention recited in Applicant's claims. Forbes specifically teaches that using the high-K dielectric to transfer charge provided benefits:

> [0023] The lower tunneling barrier height of high-k dielectric gate insulators provides larger tunneling current into the floating gate 105 with a smaller gate voltage. Additionally, larger tunneling current out of the floating gate is accomplished with smaller control gate 109 voltages.
>
> [0024] Another advantage of high-k gate insulators is that smaller write and erase voltages are necessary due to the reduced thickness of the SiO_2 layer 107 between the control gate 109 and the floating gate 105. This layer can be made less than 15 Å thick ... [Forbes, ¶¶23 and 24].

As can be seen, Forbes asserts that the reason to use the high-K dielectric includes the benefits received when transferring charge (programming/writing or erasing). Thus, one skilled in the art attempting to combine the teaching of Forbes with the teaching of Hazani would be motivated to add the high-k material of Forbes to the dielectric that will be used for transferring charge. Thus, one of ordinary skill in the art would not be motivated and there is no teaching or suggestion to alter the prior art to create a structure that includes "a first dielectric region between said channel region and said floating gate, said first dielectric region includes a high-K material; and a second dielectric region between said floating gate and said control gate, wherein charge is transferred between said floating gate and said control gate via said second dielectric region," as recited in claim 1. Therefore, Applicant asserts that claim 1, and all claims that depend from claim 1, are patentable over the prior art.

For the same reasons as described with respect to claim 1, Applicant asserts that claims 20-44 are also patentable over the prior art.

III. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-44 and 52-53 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to the outstanding Office Action.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this document, including any fee for extension of time, which may be requested.

Respectfully submitted,

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